NUMI Off-Axis Workshop
Stanford Meeting

Electronics for Digital Calorimetry

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Outline:

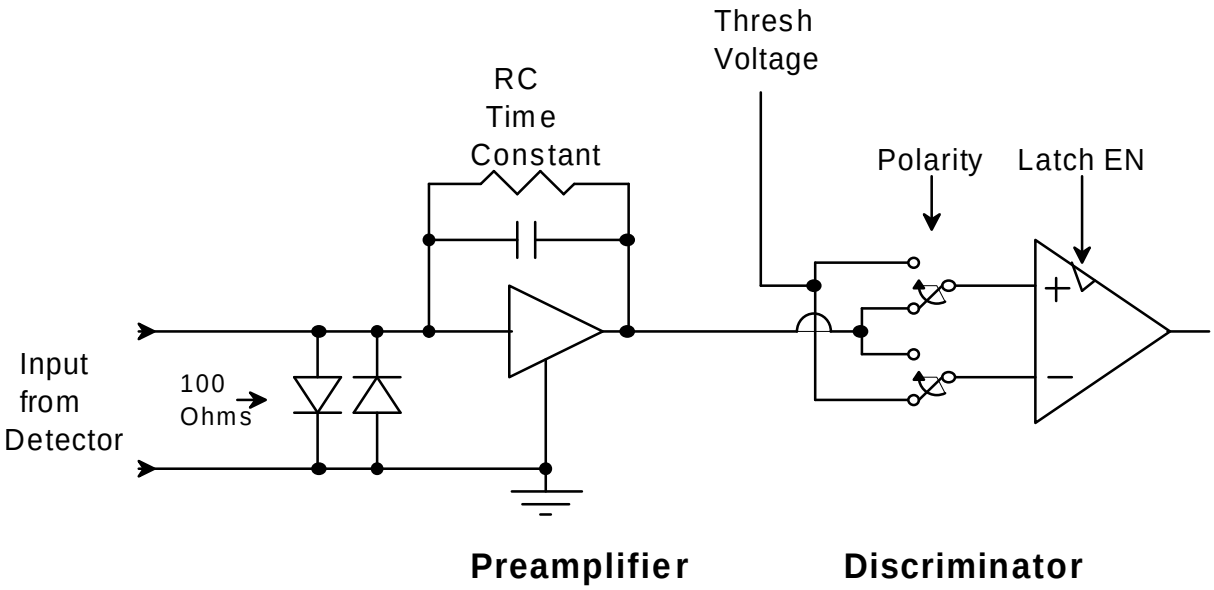
I. General Concepts
II. Description of System Components
III. Physical Configuration
IV. Cost Estimate
V. Custom IC Development

I. General Concepts

- **Develop a Custom Front-End ASIC, Which Services Many Detector Channels (64 → 128)**

- **Each Channel has a Discriminator**
  - **A 1-Bit ADC!**

- **Each Channel has a Preamplifier**
  - **Needed for Avalanche Mode**
  - **Can Bypass if Desired (→ Streamer Mode)**
  - **Provides Pulse Shaping**



Block Diagram of Front End Amplifier (FEA)

I. General Concepts (Cont.)

- **To Trigger, or Not-to-Trigger?**
  - ***No* Trigger:**
    - **Timestamp Counter Running Inside Front End Chip**
    - **Discriminator Output Latches Value of Timestamp**
    - **Store Timestamps in Local Buffers, Read Out Periodically**
    - **Read Out Timestamps into Trigger Processor**
    - **Use Timestamps to Reconstruct Hits**

    - **Simple Architecture**

    - **Works Well for Low Event Rates *and* Low Background & Noise Rates**

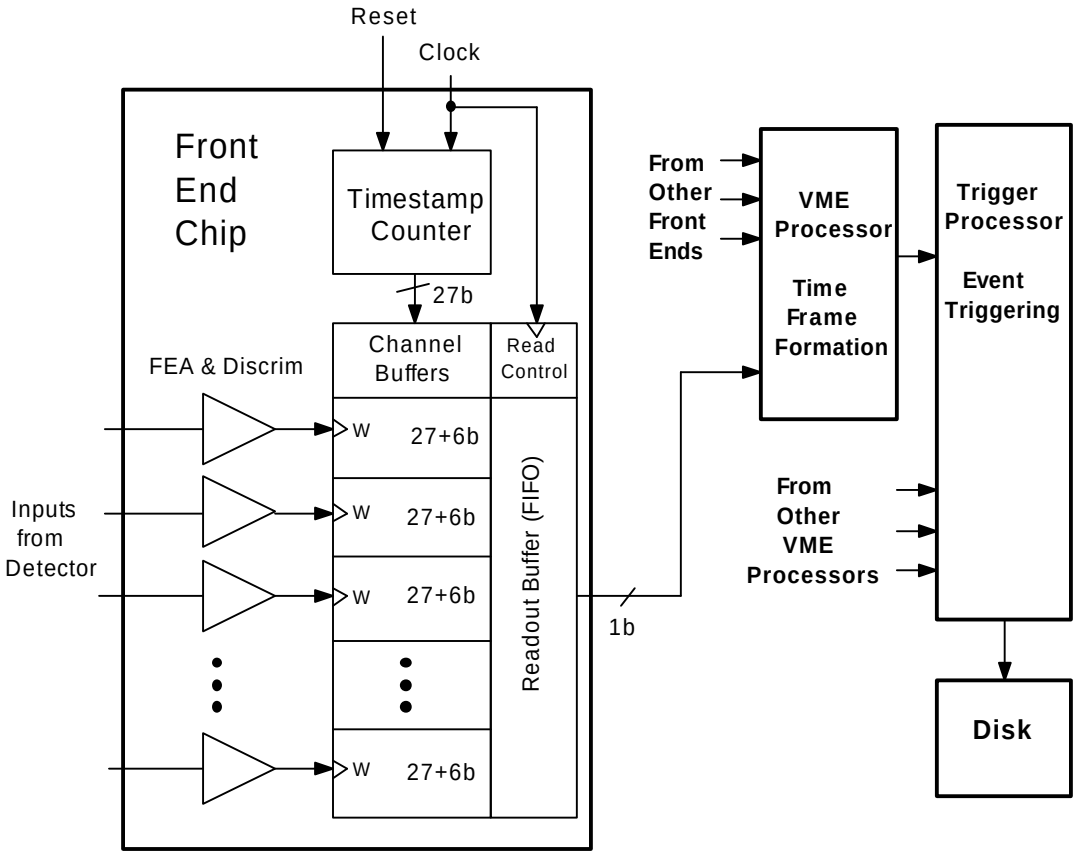
    - **Like MINOS DAQ**

    - **Might Be a Problem for Detectors on Surface…**

    - **Might Be a Problem for a Testbeam…**

I. General Concepts (Cont.)

- **To Trigger, or Not-to-Trigger (Cont)?**
  - ***No* Trigger (Cont):**



Block Diagram of *Triggerless* System

I. General Concepts (Cont.)

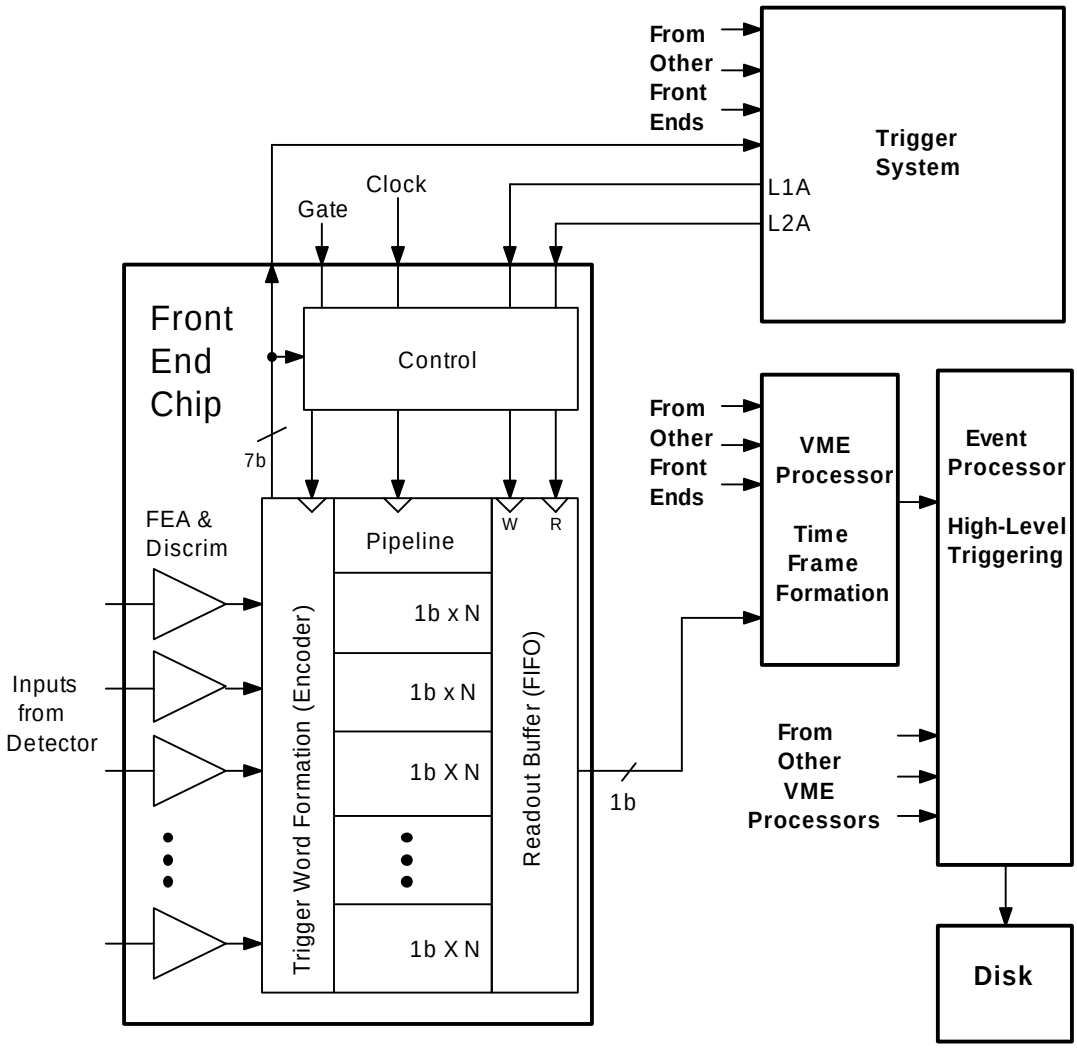
- **To Trigger, or Not-to-Trigger (Cont.)?**
  - ***With* Trigger:**
    - **Latch Outputs of All Discriminators on Each Clock Cycle, At Whatever Frequency Desired**
    - **Put "Data Word" Into Pipeline**
    - **Provide "L1" Trigger *N* nS Later to Capture data Word at End of Pipeline**
    - **Store Data Word in Local Buffers, Read Out Periodically ("L2" Trigger…)**
    - **Read Out Data into Higher-Level Trigger Processor to Perform Pattern Recognition**

    - **Chip Can Provide Trigger Output, Based on Multiplicity of Hits in a Given Clock Period**

    - **Preferred for Higher Rate Environments, or Multiple Detector Systems**

I. General Concepts (Cont.)

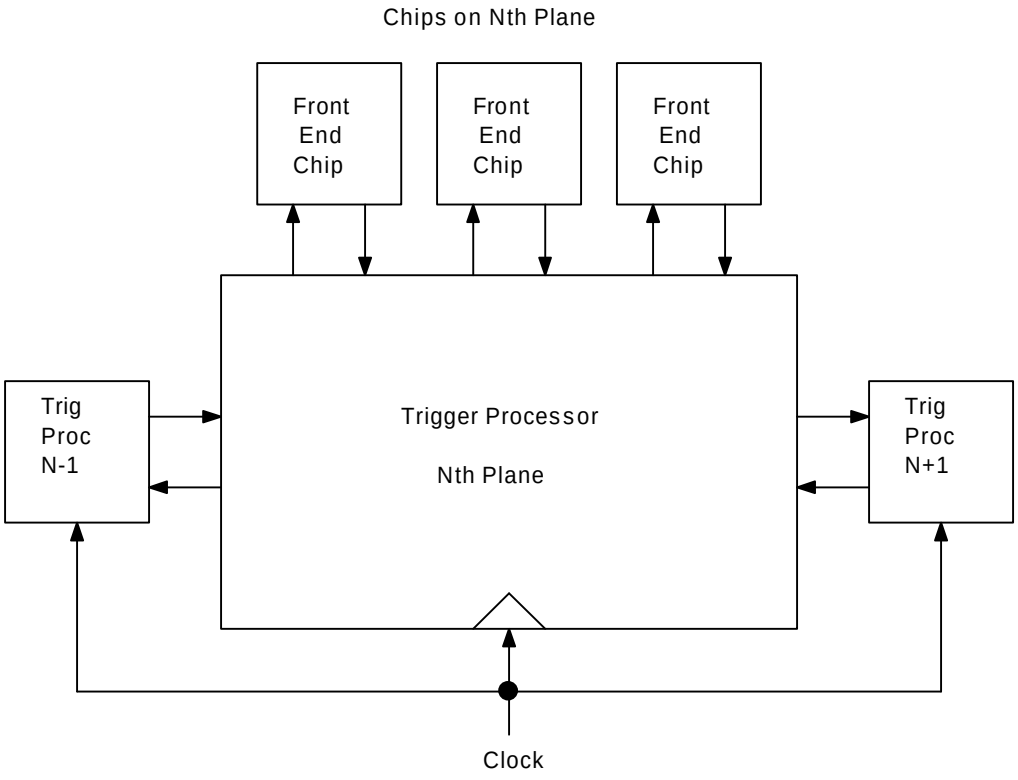
- **To Trigger, or Not-to-Trigger (Cont)?**
  - ***With* Trigger (Cont):**



Block Diagram of *Triggered* System

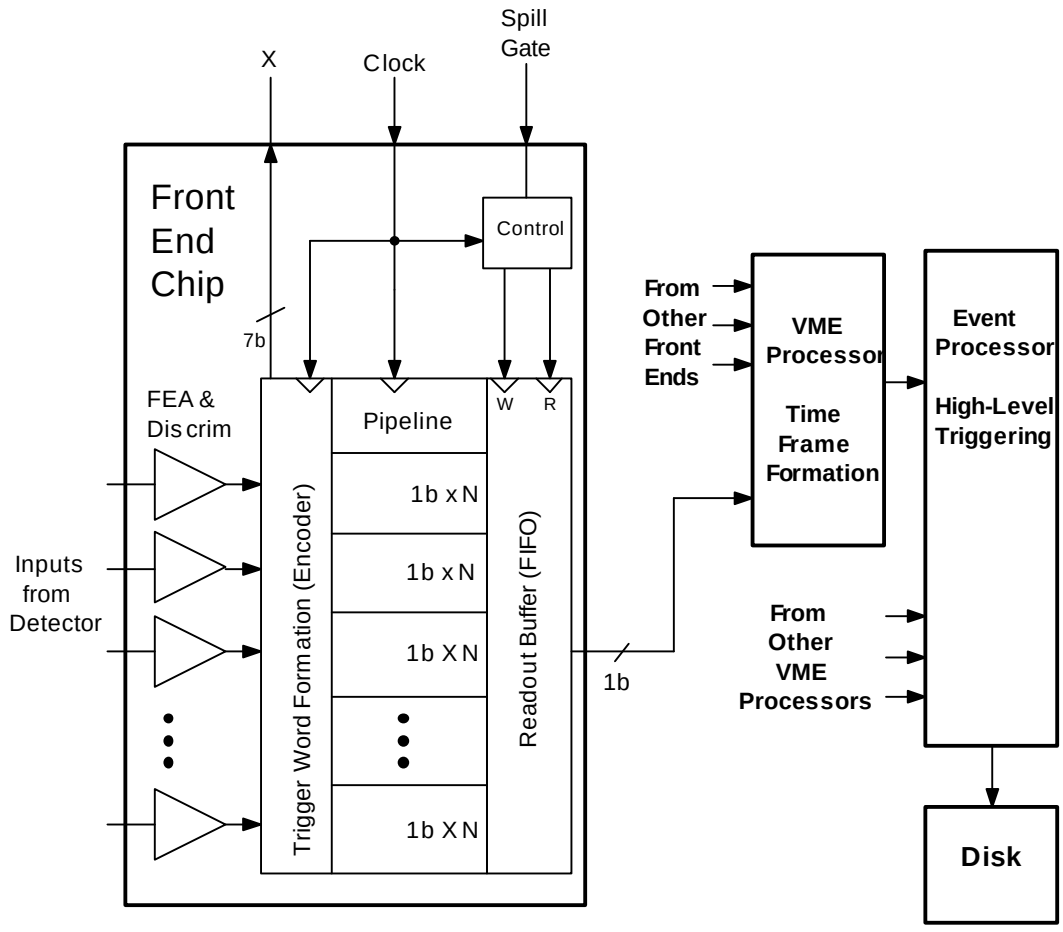
I. General Concepts (Cont.)

- **To Trigger, or Not-to-Trigger (Cont)?**
  - ***With* Trigger (Cont):**
    - **Could Arrange for Distributed "Local" Trigger, Looking for Multiplicity in Adjacent Planes Only**



I. General Concepts (Cont.)

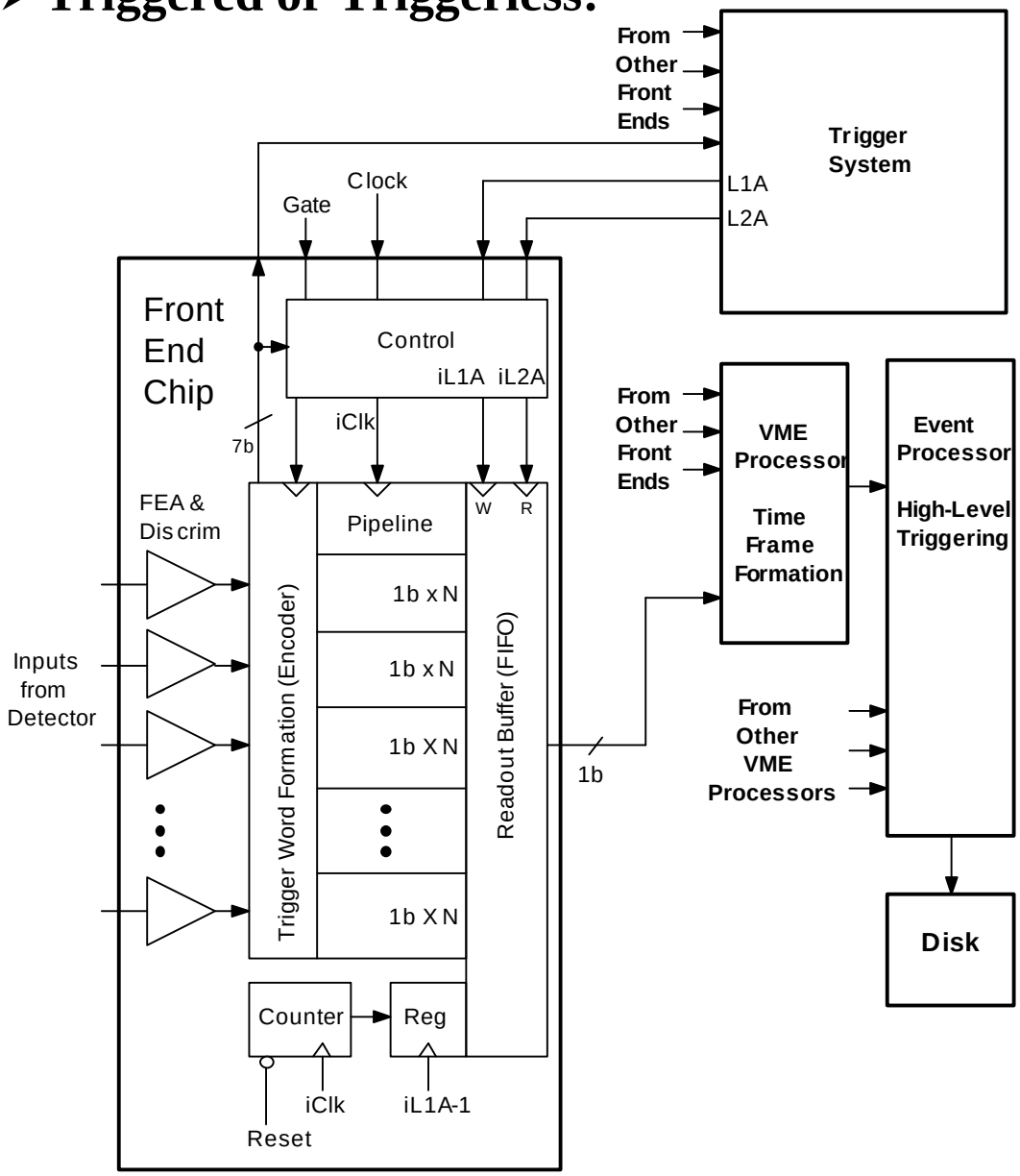
- **Variation on Triggered Architecture: Gate on Spill**
  - **No Trigger**
  - **Record All Events During Spill Period**
  - **Trigger Processor Does Sorting**
  - **Use "Pseudo-Spill" Signal to Capture Cosmic Rays**



Block Diagram of *Gated* System

I. General Concepts (Cont.)

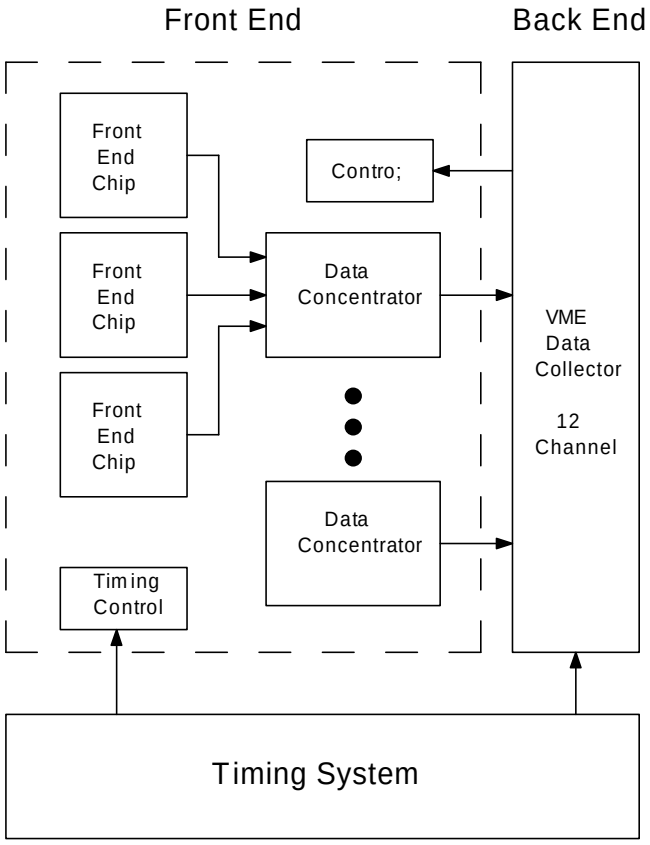
- **Variation on Triggered Architecture: Add Timestamp to Data Word**
  - **Desirable for Linear Collider RPC Detector**
  - **Triggered or Triggerless!**



II. System Components

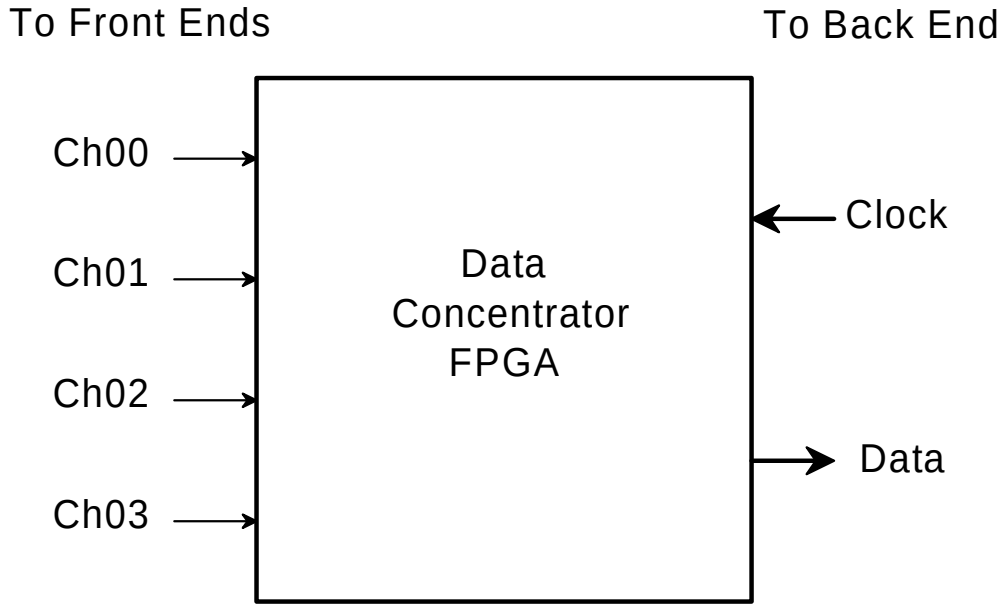
- **Basic System Architecture:**
  - ***RPC ASIC* Resides *ON* Detector**
  - ***Data Concentrator* Funnels Data From Several Front End Chips**
  - ***VME Data Collector* Funnels Data from Several Data Concentrators**

  ➢ **Goal: Reduce Number of Expensive VME Crates & Cards**



II. System Components (Cont.)

- **Data Concentrator:**
  - **To Reduce Back-End Costs, Need Intermediate Data Concentration on Detector**
  - **Multiplex Data from Several Chips into a Data Stream**
  - **Realization: FPGA**



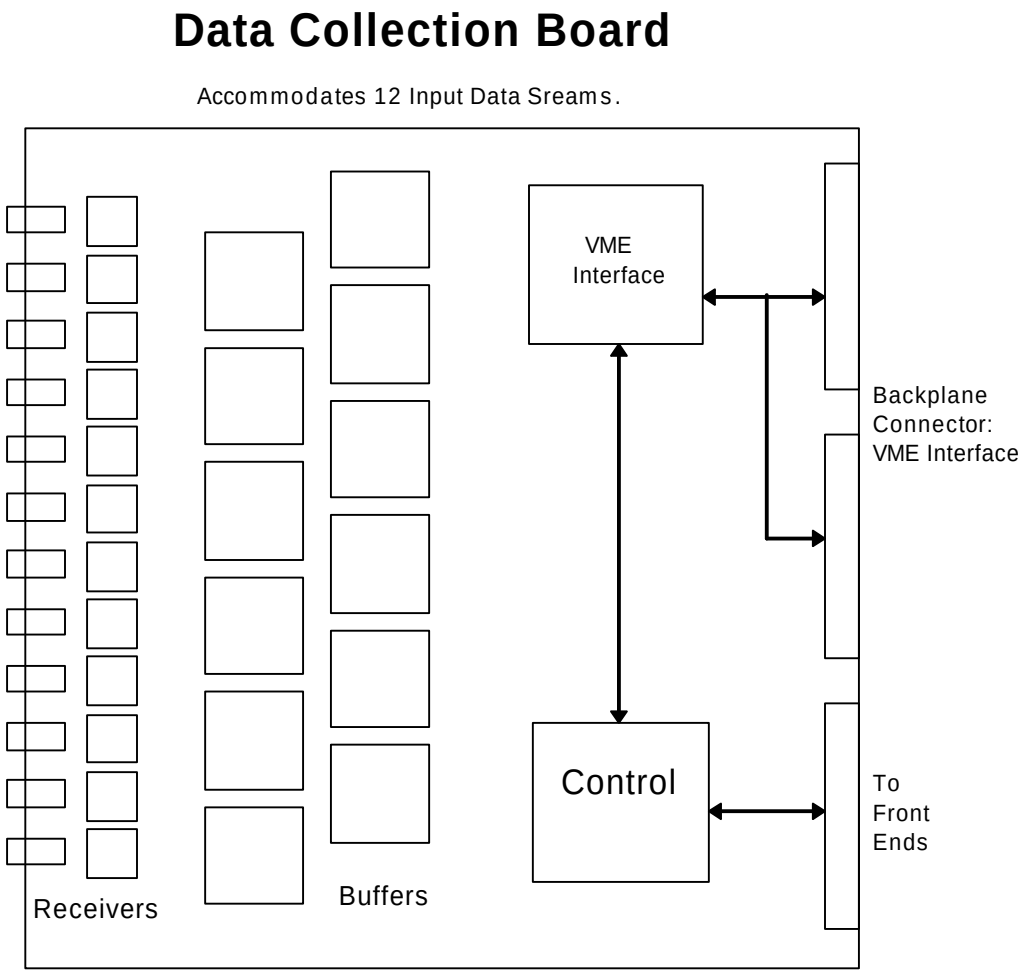
Block Diagram of Data Concentrator FPGA

II. System Components (Cont.)

- **Back End Readout:**
  - **Receive Serial Data Streams from Front End Data Concentrators**
  - **Collect Data**
  - **Form "Time Frames" (~1 Sec for MINOS)**
  - **Send Data to Trigger Processor**
  - **Realization**
    - **Use VME Crates for Infrastructure**
    - **Data Collectors Receive Serial data Streams from Front Ends**
    - **Data Collectors Also Provide Clock & Control**

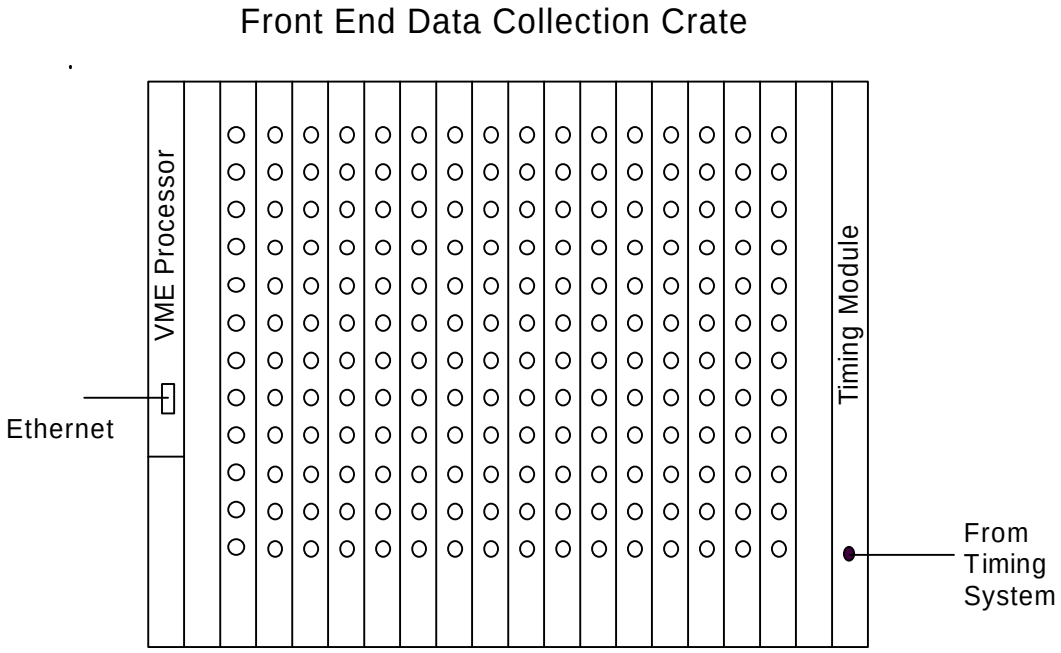
II. System Components (Cont.)

- **Back End Readout (Cont.):**
  - **Conceptual Design of Data Collection: 9U x 400 mm VME, 12 Inputs**



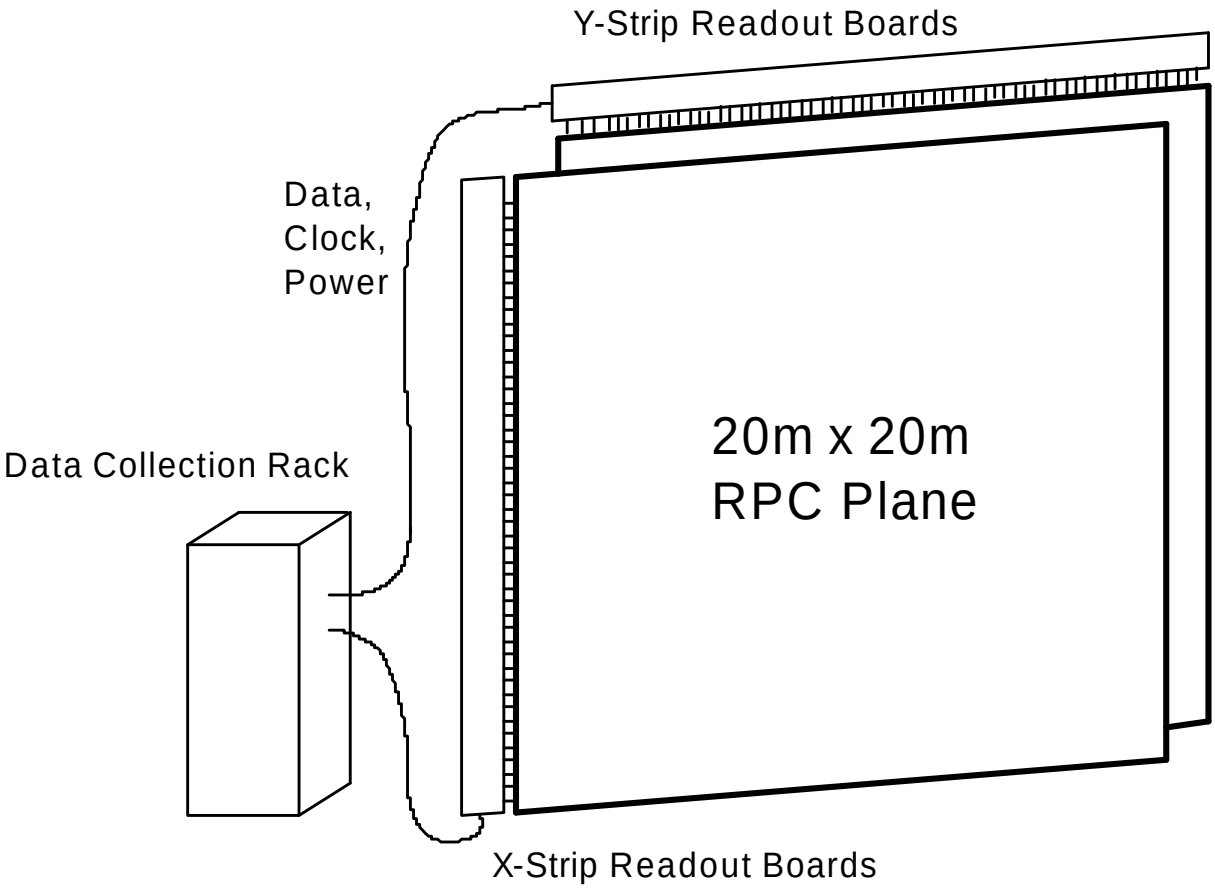
II. System Components (Cont.)

- **Back End Readout (Cont.):**
  - **Conceptual Design of Data Collection Crate: 9U x 400 mm VME, 21 Slot**



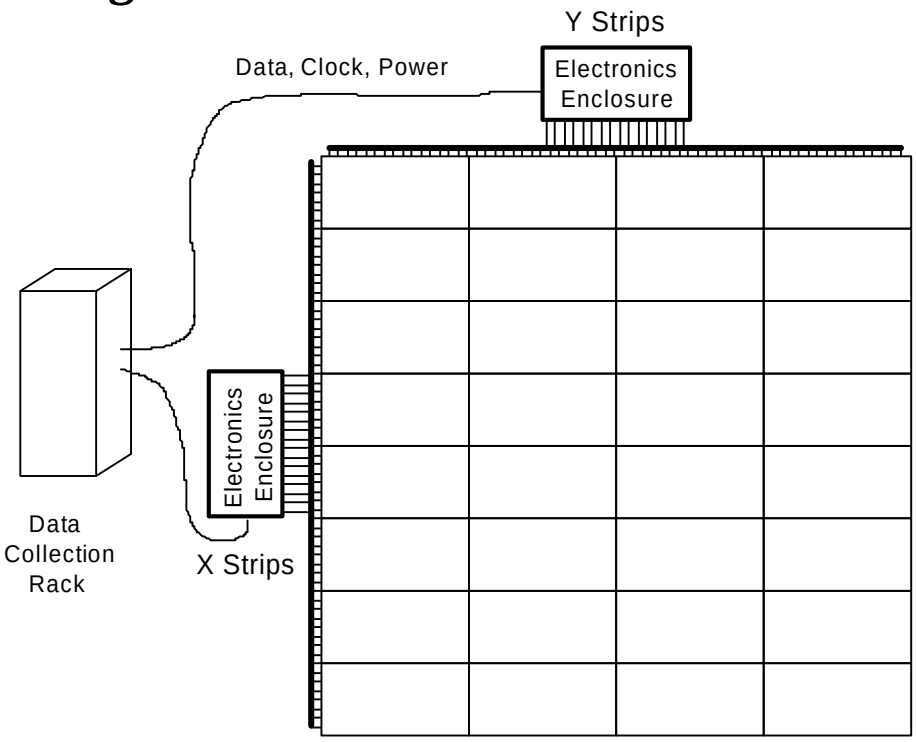
III. Physical Configuration

- ***Minimal*** **Electronics: 20 Meter Strips**
  - **Readout Boards:**
    - **Host On-Board Custom IC**
    - **Terminate Strip Transmission Lines**
    - **Distribute Power & Ground for Chip**
    - **Provide Means for Clock & Control**
    - **Host Data Concentrators**



III. Physical Configuration (Cont.)

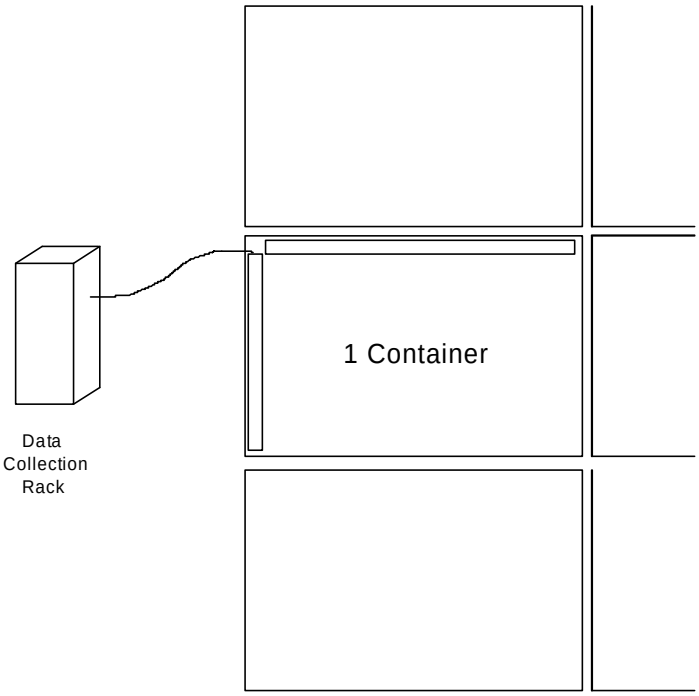
- ***Minimal*** **Electronics: 20 Meter Strips (Cont.)**
  - **Using Containers:**



- **Advantages:** **Reduces Infrastructure**
  Reduces # Channels & Cost
  Coalesces Plane Data
  Electronics Easy to Access
  Power Not a Problem
- **Disadvantages:** **Longer Signal Cables**
  Increased Capacitance
  Increased Noise
  Messy Module Interconnects

III. Physical Configuration (Cont.)

- ***Compartmentalized*** **Electronics: Self Contained**
  - **Using Containers:**



- **Advantages:** **Short Signal Cables**
  Decreased Capacitance
  Decreased Noise (Faraday!)
  No Module Interconnects
  Self Contained – Stack 'n Go!
- **Disadvantages:** **Increased Infrastructure**
  Increases # Channels & Cost
  Data Not Grouped by Plane
  Electronics Hard to Access
  Power Could Be a Problem
  Increased Dead Space

IV. Costs

- **Minimal Electronics Configuration:**
  - **64 Channel ASICs**
  - **600 Planes, 400,000 Channels Total**
  - **3 Front End Boards/Plane, 256 CH Each**
  - **12 Inputs/Data Collector → 3072 CH Each**

  - **8000 Chips (with Yield)**
  - **2000 Front End Boards**
  - **100 Front End Electronics Enclosures**
  - **180 Data Collectors**
  - **8 VME Crates**

ITEM	Unit Cost	Number Needed	Subotal
64-Ch ASICs	$25	8,000	$ 200 K
Front End Boards	$700	2,000	$ 1400 K
FE Enclosures	$500	100	$ 50 K
FE Power & Cables	$500	100	$ 50 K
Data Collectors	$3000	180	$ 540 K
VME Crates, Power, & Processors	$5000	10	$ 50 K
Trigger Processor	$20,000	1	$ 20 K
Cables, Misc	$100	1,600	$ 160 K
Total	$6.18	400,000	$2470 K

IV. Costs (Cont.)

- **Compartmentalized Electronics Configuration:**
  - **64 Channel ASICs**
  - **80 X Ch/Module, 200 Y Ch/Module**
  - **2 Chips/X Plane, 3 Chips/Y Plane, →5/Plane**
  - **10 Modules/Container, 992 Containers**
  - **50 Chips/Container, 3200 CH/Container**
  - **3.2M Front End Channels!**
  - **2 Front End Boards/Mod, 39,680 Total**
  - **5 Readout Streams/Container, 640 CH Each**
  - **12 Inputs/Data Collector → 7680 CH Each**

  - **65K Chips (with Yield)**
  - **40K Front End Boards**
  - **100 Front End Electronics Enclosures**
  - **450 Data Collectors**
  - **21 VME Crates**

ITEM	Unit Cost	Number Needed	Subotal
64-Ch ASICs	$25	65,000	$ 1625 K
Front End Boards	$100	40,000	$ 4000 K
FE Power & Cables	$500	1000	$ 500 K
Data Collectors	$3000	450	$ 1350 K
VME Crates, Power, & Processors	$5000	21	$ 105 K
Trigger Processor	$20,000	1	$ 20 K
Cables, Misc	$100	1,000	$ 100 K
Total	$2.41	3,200,000	$7700 K

V. Custom Integrated Circuit Development

- **Development Being Pursued for Linear Collider Digital HCAL (RPCs)**
  - **Requirements Similar**
  - **Have Some Funding, Additional Being Pursued**
  - **Have Been Discussing Development with ASIC Design Groups (FNAL Included…)**
    - **Reaction & Enthusiasm *Positive***
- **Logistics:**
  - **Development Time for First Prototype ~6 Mo. – 1 Year**
  - **Need Clear Definition of Functionality**
  - **Chip Not Difficult, But Has Many Blocks**
  - **Probably Can Use Prototype Fab Services to Start (~2 Dozen Chips, ~3 Months, ~$15K)**
  - **For Production (~500K – 3.2M Channels), Cost of Custom IC Design & Fab *Will Be Worth It* (~$0.50 /Channel for Chip)**